

(12) **United States Patent**
Godo et al.

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(54) **MANUFACTURING METHOD AND TEST METHOD OF SEMICONDUCTOR DEVICE**

(58) **Field of Classification Search**
None
See application file for complete search history.

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi, Kanagawa-ken (JP)

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(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi, Kanagawa-ken (JP)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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This patent is subject to a terminal disclaimer.

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Primary Examiner — Calvin Choi

Related U.S. Application Data

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(74) *Attorney, Agent, or Firm* — Eric J. Robinson; Robinson Intellectual Property Law Office, P.C.

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(57) **ABSTRACT**

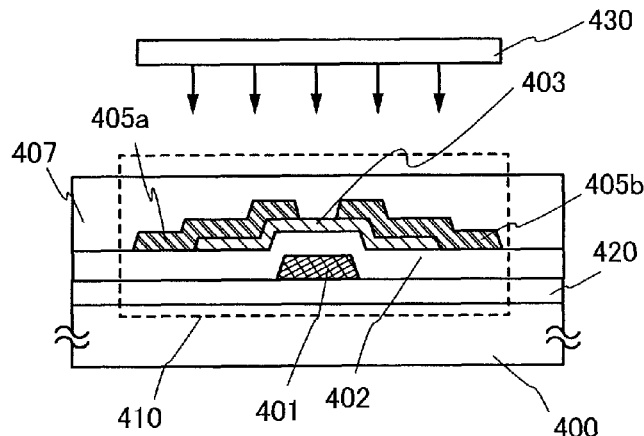
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(Continued)

Provided is a test method by which a transistor whose reliability is low can be detected with low stress and high accuracy in a shorter period of time than a BT test. Provided is to detect a transistor whose reliability is high in a shorter period of time than a BT test and manufacture an electronic device with high reliability efficiently. Hysteresis characteristics revealed in the result of the Vg-Id measurement with light irradiation to the transistor correlate with the result of a BT test; whether the reliability of the transistor is Good or Not-Good can be judged. Accordingly, the test method by which a transistor whose reliability is low can be detected with low stress and high accuracy in a shorter period of time than a BT test can be provided.

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CPC **H01L 22/14** (2013.01); **G01R 31/2625** (2013.01); **H01L 29/66969** (2013.01); **H01L 29/7869** (2013.01); **G01R 31/311** (2013.01)

9 Claims, 10 Drawing Sheets



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FIG. 1A

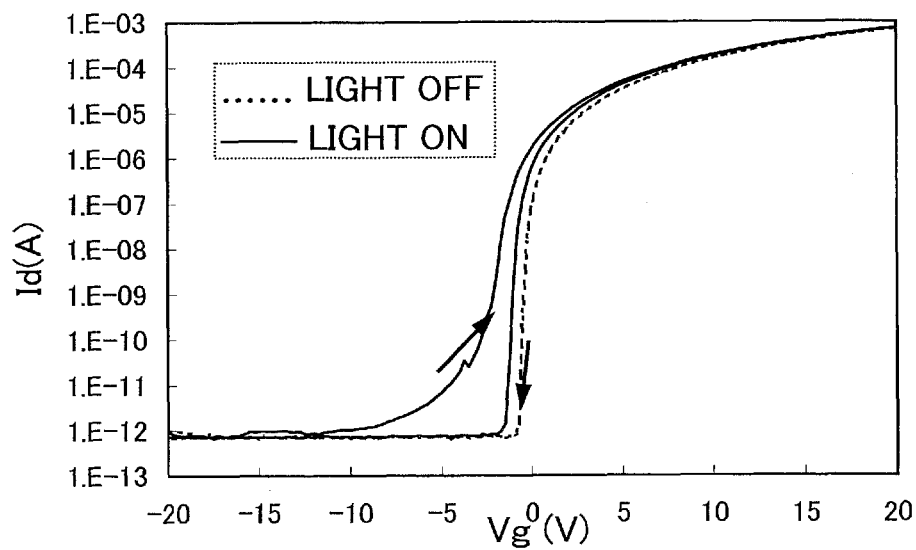


FIG. 1B

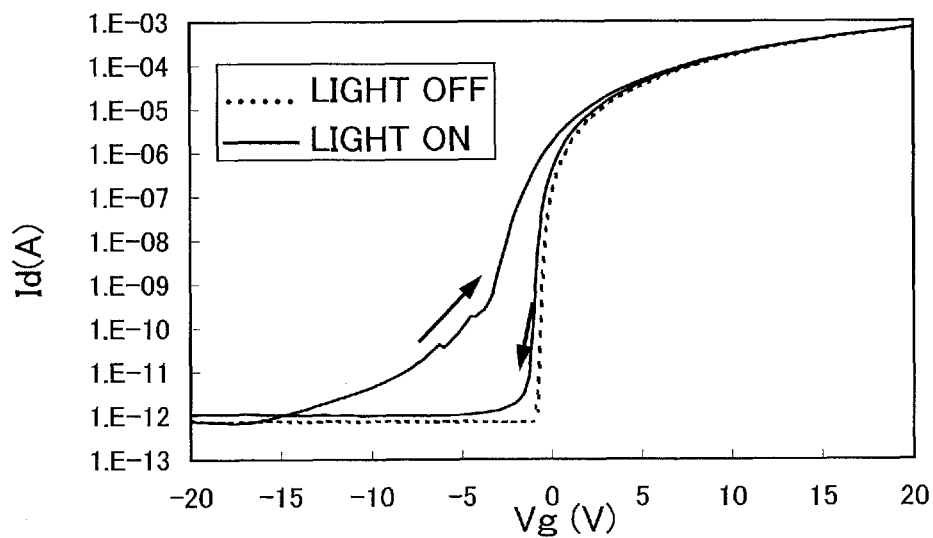


FIG. 2

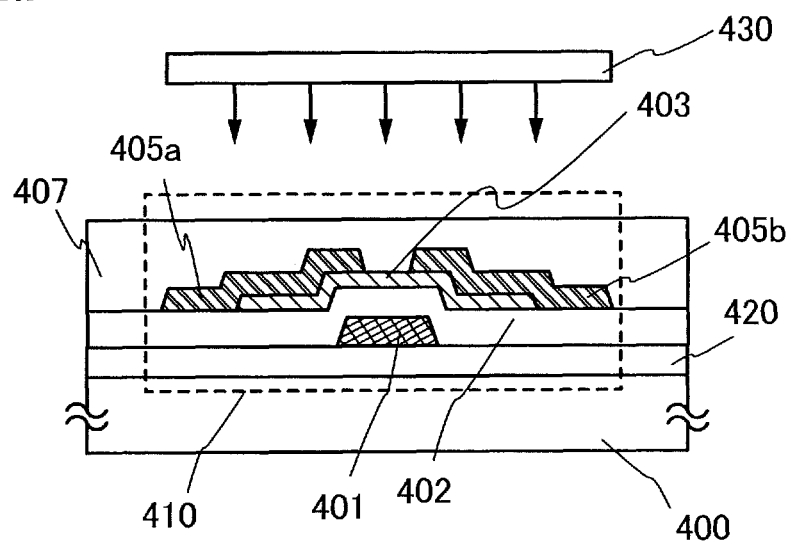


FIG. 3

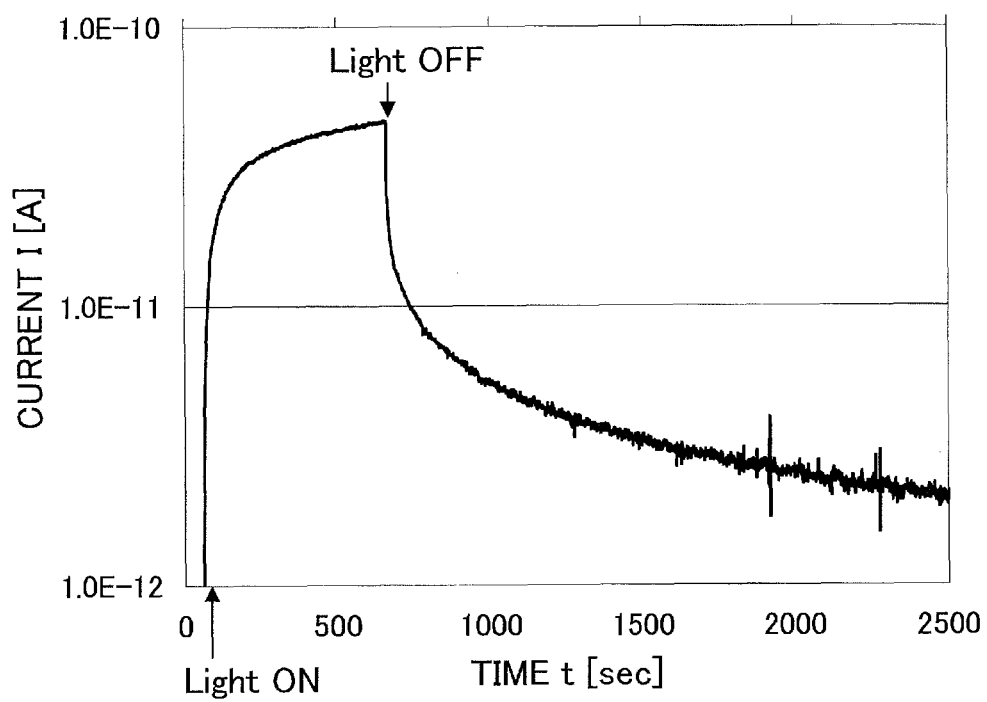


FIG. 4A

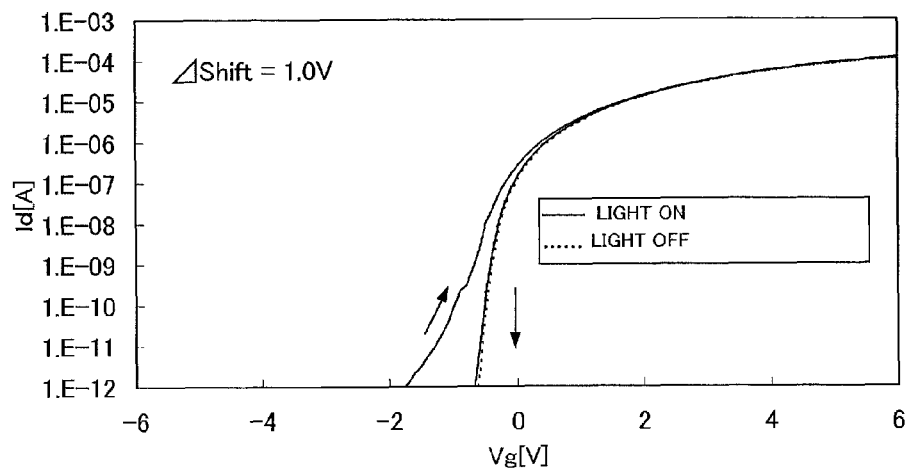


FIG. 4B

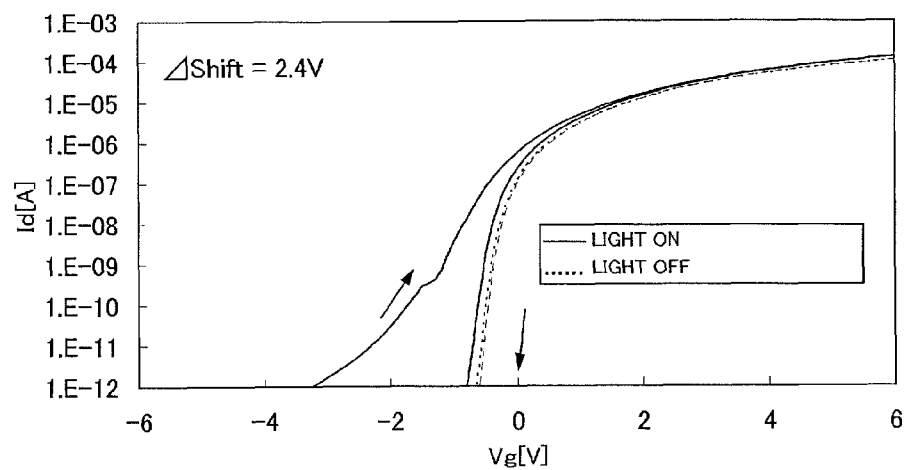


FIG. 4C

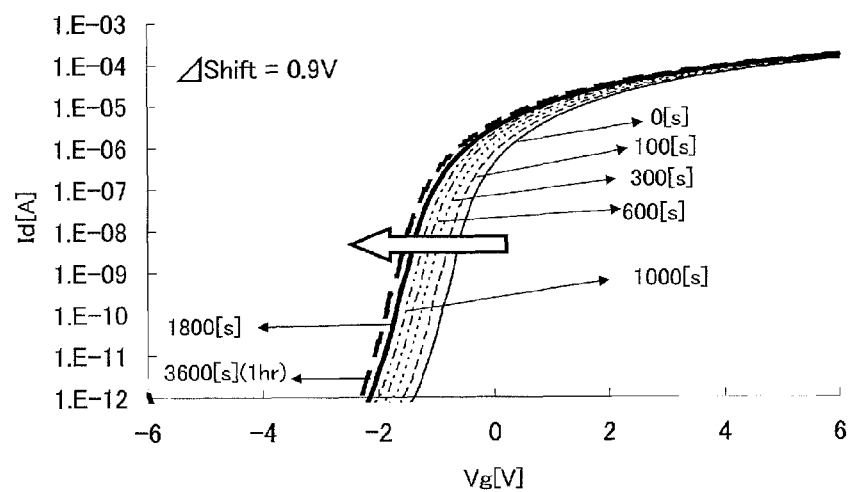


FIG.5A

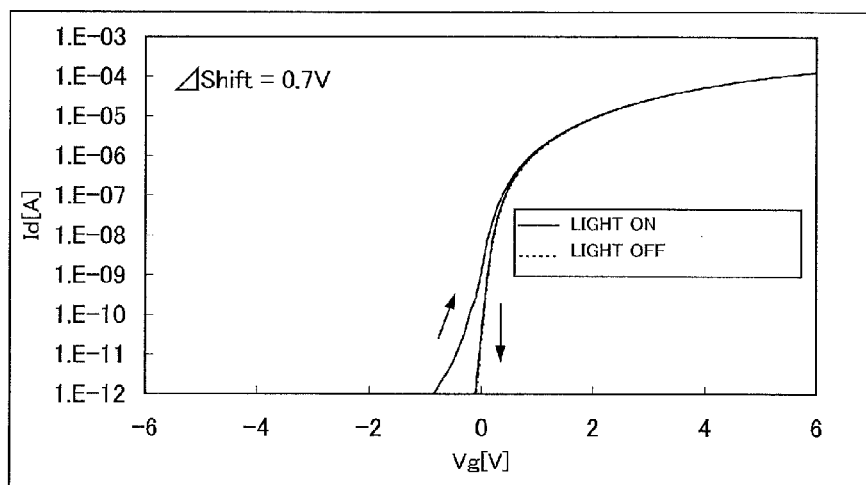


FIG.5B

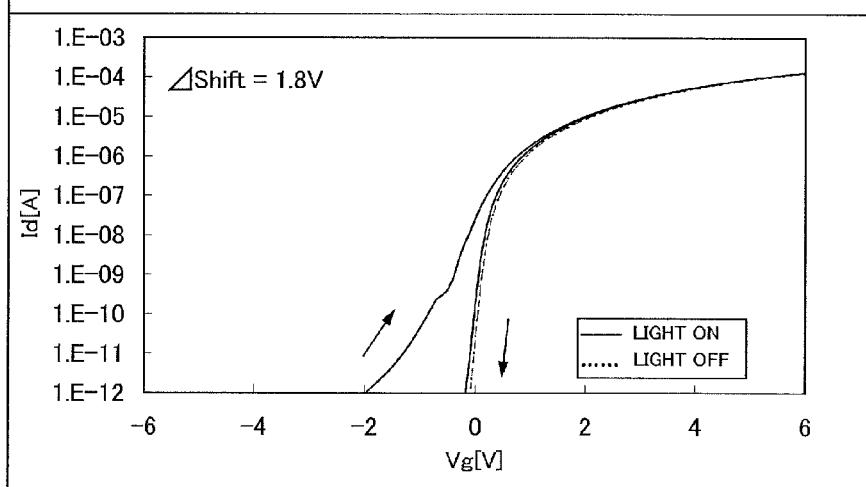


FIG.5C

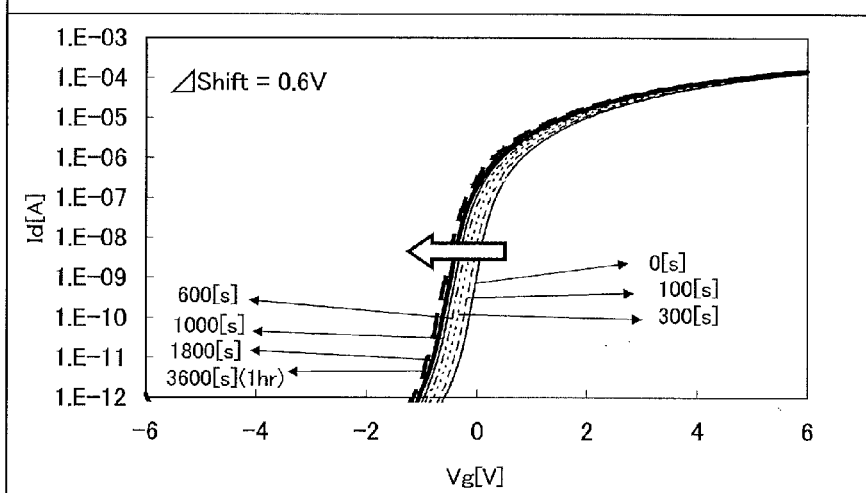


FIG. 6A

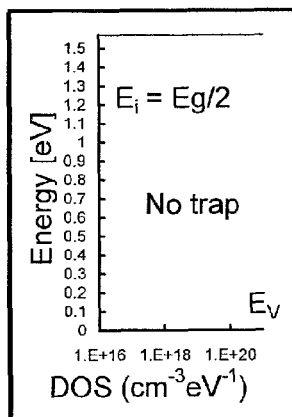


FIG. 6B

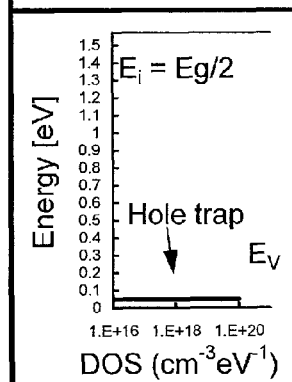


FIG. 6C

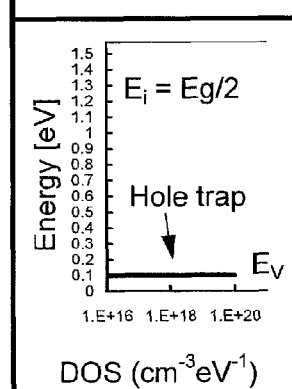
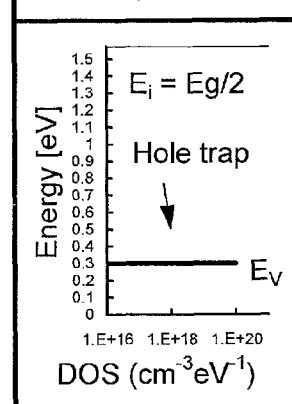


FIG. 6D



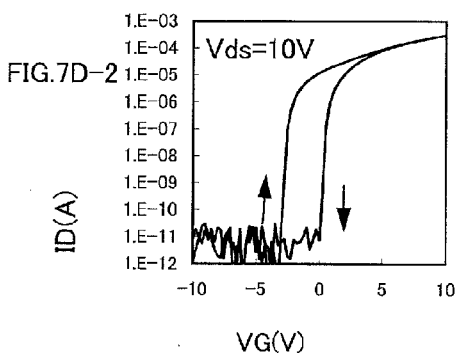
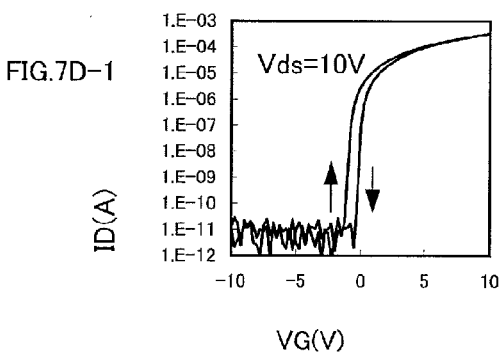
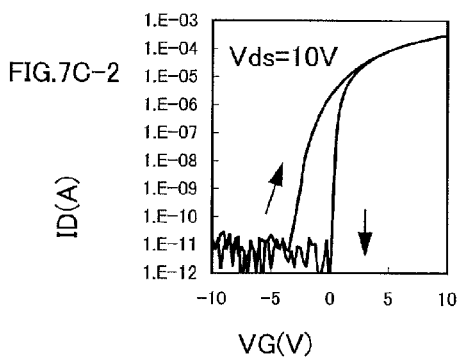
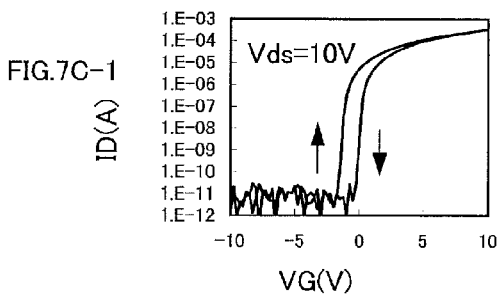
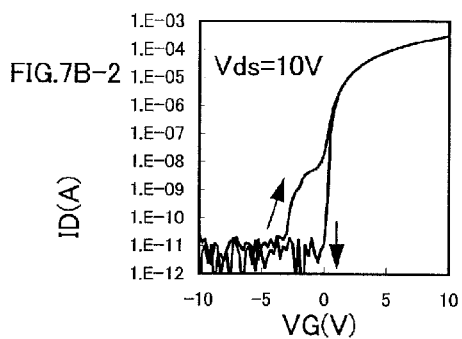
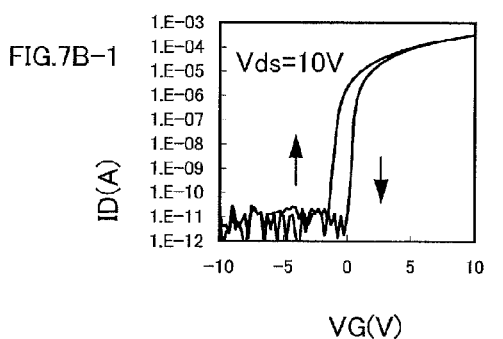
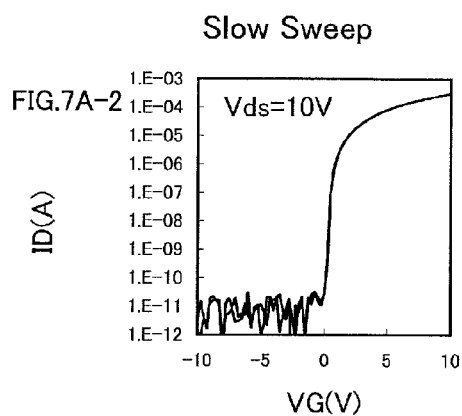
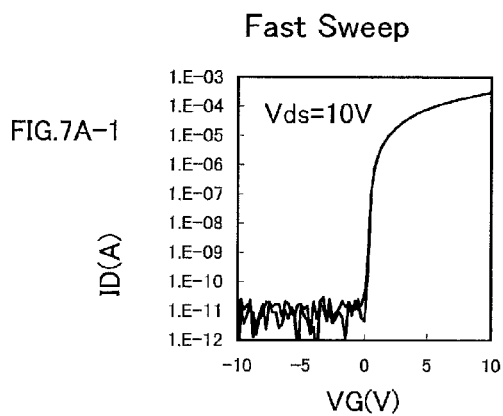


FIG. 8

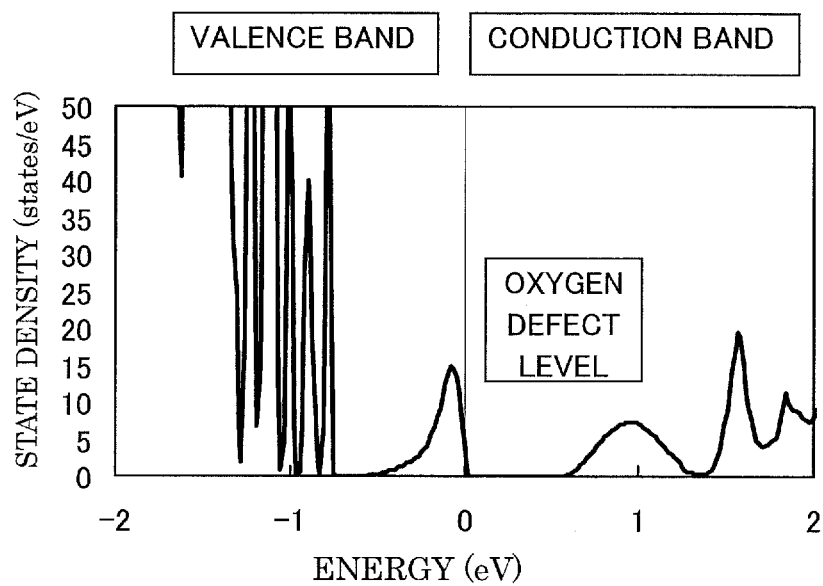


FIG. 9

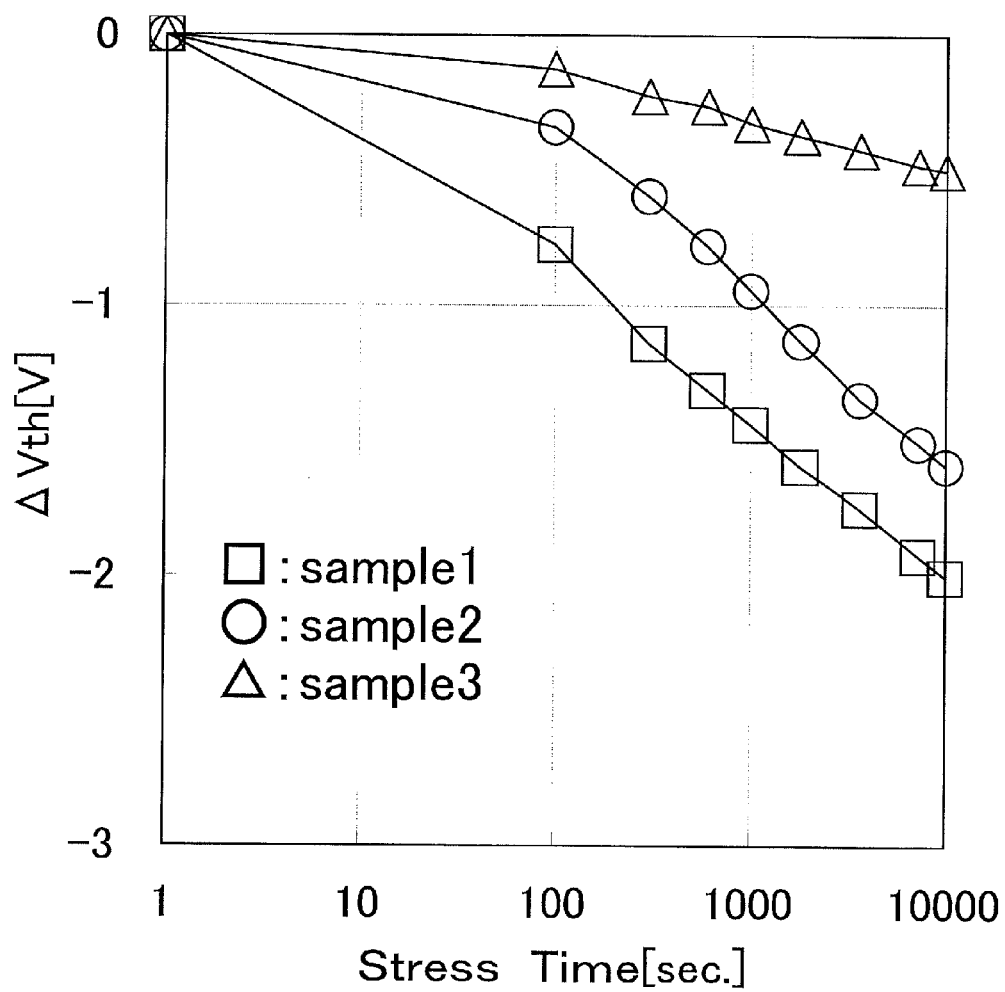


FIG. 10A

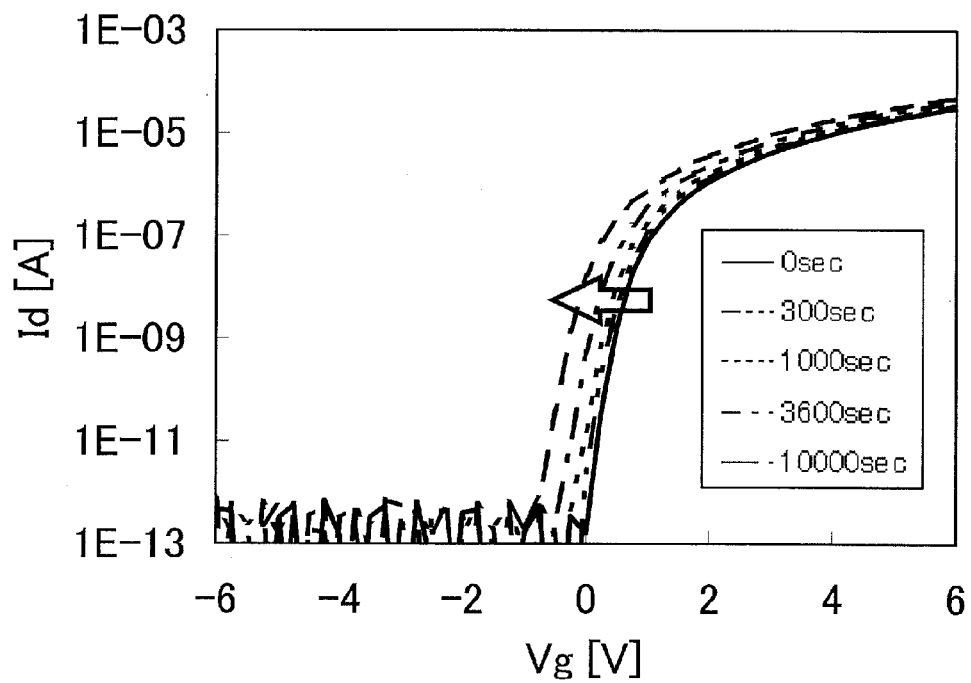
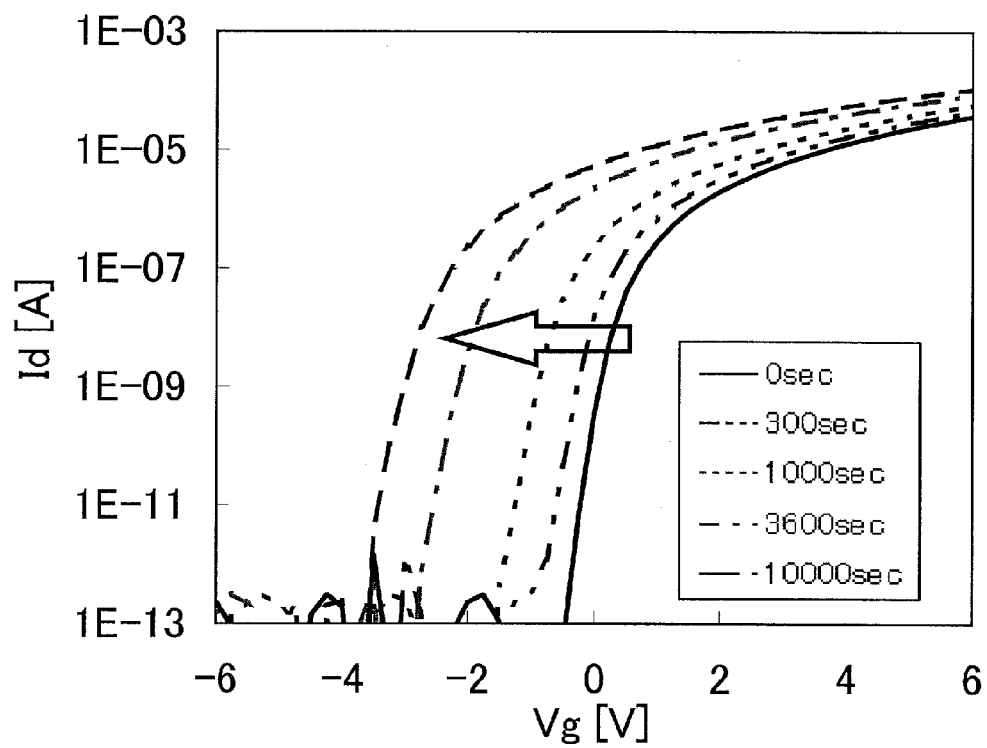


FIG. 10B



1

MANUFACTURING METHOD AND TEST METHOD OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a manufacturing method of a semiconductor device including a circuit including a transistor and a test method of the semiconductor device. The present invention relates to an electronic device equipped with a display device using an active element which is, for example, an active element including an oxide semiconductor, as a semiconductor element.

In this specification, a semiconductor device generally means any device which can function by utilizing semiconductor characteristics; an electrooptic device, a semiconductor circuit, and an electronic device are all included in the category of the semiconductor device.

2. Description of the Related Art

Although transistors using amorphous silicon have been used for conventional display devices typified by liquid crystal televisions, an oxide semiconductor has attracted attention as a material which replaces a silicon semiconductor. For example, an active matrix display device in which an amorphous oxide including In, Ga, and Zn is used for an active layer of a transistor and the electron carrier concentration of the amorphous oxide is lower than $10^{18}/\text{cm}^3$ is disclosed (see Patent Document 1).

However, there have been some problems in such a transistor using an oxide semiconductor. One of the problems is the stability of the characteristics; it has been pointed out that the electric characteristics of the transistor are changed by irradiation with visible light or ultraviolet light.

REFERENCE

Patent Document 1: Japanese Published Patent Application No. 2006-165528

SUMMARY OF THE INVENTION

End-product reliability of an electronic device using a plurality of transistors has not been assured in some cases where at least one of the transistors does not meet the certain standard on the shift amount of the threshold voltage by voltage stress.

One of test methods for examining reliability of a transistor is a bias-temperature stress test (hereinafter, referred to as a BT test). The BT test is a kind of accelerated test, and can evaluate a change in characteristics caused by long-term usage of a transistor. The amount of shift of the threshold voltage of a transistor through the BT test is particularly an important benchmark for the reliability. The smaller the amount of shift of the threshold voltage of a transistor through the BT test is, the higher the reliability of a product including the transistor is.

Specifically, the temperature of a substrate provided with the transistor (substrate temperature) is kept at a fixed temperature, a source and a drain of the transistor are set at the same potential as each other, and a gate of the transistor is applied with a potential different from those of the source and the drain for a certain period, for example, for 1 hour. The BT test in which the potential applied to the gate is higher than the potential of the source or the drain is referred to as a +BT test and the BT test in which the potential applied to the gate is lower than the potential of the source or the drain is referred to as a -BT test.

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The BT test is performed on a transistor which has been never subjected to a BT test. For example, if a -BT test is performed on a transistor which has been once subjected to a +BT test, the results of the -BT test cannot be evaluated correctly due to influence of the previous +BT test. The same applies to the case where a +BT test is performed on a transistor which has been once subjected to a -BT test. Therefore, the BT test involves many samples and takes time.

Further, since the BT test is an accelerated test, a transistor suffers stress damage by the BT test and the transistor after being subjected to the BT test cannot be used in an end product. Therefore, it has been demanded that a Good/Not-Good test is conducted on a transistor and then, an end product is manufactured using the tested transistor; that is, a test method for evaluating and judging the reliability of a transistor, in a manufacturing process of a semiconductor device has been demanded.

One object of one embodiment of the present invention is to provide a test method by which a transistor whose reliability is low can be detected with low stress and high accuracy in a shorter period of time than a BT test.

One object of one embodiment of the present invention is to detect a transistor whose reliability is high in a shorter period of time than a BT test and manufacture an electronic device with high reliability efficiently.

One embodiment of the present invention is a test method for evaluating the reliability of a transistor. The method is also a test method of a semiconductor device, in which hysteresis characteristics of Id-Vg characteristics of a transistor, which are obtained by measuring the current (Id) between a drain electrode and a source electrode of the transistor while irradiating the transistor with light and changing the voltage (Vg) between a gate electrode of the transistor and the source electrode are analyzed.

Such hysteresis characteristics revealed in the result of the Vg-Id measurement with light irradiation to the transistor correlate with the result of a BT test; whether the reliability of the transistor is Good or Not-Good can be judged.

It is ideal that in the Vg-Id measurement with light irradiation to the transistor, a Vg-Id curve at a sweep of the gate voltage by a certain voltage from negative voltage to positive voltage be substantially coincide with a Vg-Id curve at a sweep of the gate voltage by the certain voltage from positive voltage to negative voltage.

The test for evaluating the reliability with the measurement of the electrical characteristics of a transistor with light irradiation can be applied as one step of a manufacturing process of a semiconductor device. According to a manufacturing method of a semiconductor device in that case, transistors are manufactured, Good/Not-Good judgment is conducted using Id-Vg curves of each of the transistors obtained by measuring the drain-source current (Id) of the transistor while irradiating the transistor with light and changing the gate-source voltage (Vg) of the transistor, and then, the semiconductor device is manufactured using the transistor(s) which is/are judged to be Good.

In particular, it has been confirmed that in the case where an oxide semiconductor material is used for a semiconductor layer of a transistor, a -BT test, i.e., application of a negative gate stress, with light irradiation accelerates the degradation of the transistor to make the transistor be in the normally-ON state. This degradation is also called negative-bias temperature stress photodegradation.

A transistor exhibiting large negative-bias temperature stress photodegradation shows a large difference between a Vg-Id curve at a sweep of the gate voltage from negative voltage to positive voltage by a certain voltage (e.g., 0.25 V)

and a V_g - I_d curve at a sweep of the gate voltage from positive voltage to negative voltage by the certain voltage.

On the other hand, a transistor exhibiting small negative-bias temperature stress photodegradation tends to show a small difference between a V_g - I_d curve at a sweep of the gate voltage from negative voltage to positive voltage by a certain voltage and a V_g - I_d curve at a sweep of the gate voltage from positive voltage to negative voltage by the certain voltage.

In this specification, an oxide semiconductor material means a four-component metal oxide such as an In—Sn—Ga—Zn—O-based oxide semiconductor; a three-component metal oxide such as an In—Ga—Zn—O-based oxide semiconductor, an In—Sn—Zn—O-based oxide semiconductor, an In—Al—Zn—O-based oxide semiconductor, a Sn—Ga—Zn—O-based oxide semiconductor, an Al—Ga—Zn—O-based oxide semiconductor, or a Sn—Al—Zn—O-based oxide semiconductor; a two-component metal oxide such as an In—Zn—O-based oxide semiconductor, a Sn—Zn—O-based oxide semiconductor, an Al—Zn—O-based oxide semiconductor, a Zn—Mg—O-based oxide semiconductor, a Sn—Mg—O-based oxide semiconductor, an In—Mg—O-based oxide semiconductor, or an In—Ga—O-based oxide semiconductor; an In—O-based oxide semiconductor, a Sn—O-based oxide semiconductor, or a Zn—O-based oxide semiconductor; or the like. Further, SiO_2 may be contained in the above oxide semiconductor. Here, for example, an In—Ga—Zn—O-based oxide semiconductor means an oxide containing indium (In), gallium (Ga), and zinc (Zn), and there is no particular limitation on the composition ratio thereof. The In—Ga—Zn—O-based oxide semiconductor may contain an element other than In, Ga, and Zn.

In the case where an In—Zn—O-based material is used as an oxide semiconductor, a target therefore has a composition ratio of In:Zn=50:1 to 1:2 in atomic ratio (In_2O_3 :ZnO=25:1 to 1:4 in molar ratio), preferably In:Zn=20:1 to 1:1 in atomic ratio (In_2O_3 :ZnO=10:1 to 1:2 in molar ratio), further preferably In:Zn=15:1 to 1.5:1 in atomic ratio (In_2O_3 :ZnO=15:2 to 3:4 in molar ratio). For example, in a target used for formation of an In—Zn—O-based oxide semiconductor which has an atomic ratio of In:Zn:O=X:Y:Z, the relation of $Z>1.5X+Y$ is satisfied.

According to one embodiment of the present invention, a test method by which a transistor whose reliability is low can be detected with low stress and high accuracy in a shorter period of time than a BT test can be provided.

According to one embodiment of the present invention, a transistor whose reliability is high can be detected in a shorter period of time than a BT test and an electronic device with high reliability can be manufactured efficiently.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are graphs illustrating one embodiment of the present invention.

FIG. 2 illustrates a cross-sectional structure illustrating one embodiment of the present invention.

FIG. 3 is a graph showing photoresponse characteristics.

FIGS. 4A and 4B are graphs illustrating one embodiment of the present invention, and FIG. 4C is a graph illustrating a comparative example.

FIGS. 5A and 5B are graphs illustrating one embodiment of the present invention, and FIG. 5C is a graph illustrating a comparative example.

FIGS. 6A to 6D are graphs of considering a donor trap (a trap capturing a hole) in a bandgap.

FIGS. 7A-1 and 7A-2, 7B-1 and 7B-2, 7C-1 and 7C-2, and 7D-1 and 7D-2 are graphs showing simulation results.

FIG. 8 is a graph showing a state density in an oxygen-deficient state.

FIG. 9 is a graph showing results of a -BT test.

FIGS. 10A and 10B are graphs showing results of -BT tests (Comparative Examples)

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not construed as being limited to description of the embodiments.

Embodiment 1

Described in Embodiment 1 is a relation between degradation with light irradiation to a transistor using an In—Ga—Zn—O-based oxide semiconductor which is a ternary metal oxide and hysteresis characteristics of the transistor.

First, results of a -BT test on a transistor ($L/W=3\text{ }\mu\text{m}/50\text{ }\mu\text{m}$) using an In—Ga—Zn—O-based oxide semiconductor are shown in FIG. 10A. The -BT test was conducted at a drain-source voltage (V_d) of 3 V and a gate-source voltage (V_g) of -6 V such that the intensity of an electric field applied to a gate insulating film is -2 MV/cm. The application of the negative gate stress was kept for 0 seconds, 300 seconds, 1000 seconds, 3600 seconds, and 10000 seconds, V_g - I_d curves for which showed that the V_g - I_d curve shifts in a negative direction (a direction indicated by an arrow in FIG. 10A) as the kept time gets longer.

Further, results of the -BT test with light irradiation using an LED light source (white light with 36000 lux) are shown in FIG. 10B. As compared with FIG. 10A with no light irradiation, the V_g - I_d curves shifted further in the negative direction in FIG. 10B. The substrate temperature in the -BT test was set to room temperature.

The photoresponse characteristics of the transistor using an In—Ga—Zn—O-based oxide semiconductor are shown in FIG. 3. White light with a wavelength (λ) of 400 nm was used as a light source. In FIG. 3, a timing at which the light source is turned on is indicated by an upward arrow, and a timing at which the light source is turned off after white light irradiation for 600 seconds is indicated by a downward arrow. As shown in FIG. 3, a relaxation time τ of the transistor using an In—Ga—Zn—O-based oxide semiconductor is long. The relaxation time τ depends on a model of carrier recombination. The long relaxation time τ is caused by, for example, slowness of relaxation of extinction of an electron-hole pair generated by light in the In—Ga—Zn—O-based oxide semiconductor.

The transistor using the In—Ga—Zn—O-based oxide semiconductor exhibited hysteresis characteristics in V_g - I_d characteristics measured at room temperature with irradiation with light ($\lambda=350\text{ nm}$). The results are shown in FIGS. 1A and 1B.

A cross-sectional structure of a transistor which is one embodiment of the transistor using the In—Ga—Zn—O-based oxide semiconductor, which was measured with irradiation with light ($\lambda=350\text{ nm}$) from a light source 430 is shown in FIG. 2. A transistor 410 illustrated in FIG. 2 is a bottom-gate transistor and is also called an inverted staggered transistor.

The transistor **410** includes, over a substrate **400** having an insulating surface, an insulating layer **420** including an insulating material, a gate electrode **401**, a gate insulating layer **402** including an insulating material, an oxide semiconductor layer **403**, a source electrode **405a**, and a drain electrode **405b**. Further, a buffer layer **407** including an insulating material, which covers the transistor **410** and is in contact with the oxide semiconductor layer **403** is provided.

In the Vg-Id measurement whose results are shown in FIGS. **1A** and **1B**, the gate voltage was changed (sweep) by 0.25 V from -20 V to +20 V, and then to -20 V. Two kinds of measurements were performed: the measurement in which the integration time for one step (0.25 V) was set short to change the gate voltage fast (Fast Sweep); and the measurement in which the integration time for one step was set long to change the gate voltage slowly (Slow Sweep). The results of the measurement in which the gate voltage was changed fast (Fast Sweep) are shown in FIG. **1A**, and the results of the measurement in which the gate voltage was changed slowly (Slow Sweep) are shown in FIG. **1B**. Table 1 shows respective integration times in Fast Sweep and Slow Sweep. For the convenience of a measuring equipment, the integration time for one step was changed in accordance with a drain current to be measured.

TABLE 1

Range of Drain Current	Fast Sweep	Slow Sweep
~10 pA	1 sec	2 sec
10 pA~100 pA	0.2 sec	3.2 sec
100 pA~1 nA	0.1 sec	1.6 sec
1 nA~1 A	0.02 sec	0.32 sec

The results of the Vg-Id measurement with no light irradiation are also shown in FIGS. **1A** and **1B**, in which no hysteresis characteristics are observed.

In each of FIGS. **1A** and **1B**, hysteresis characteristics are observed in the cases with light irradiation ($\lambda=350$ nm); in particular, the Vg-Id curve is shifted in a negative direction in the case at the sweep from -20 V to +20 V. In addition, the hysteresis characteristics are more apparent in Slow Sweep than in Fast Sweep.

In the Vg-Id characteristics with light irradiation in each of FIGS. **1A** and **1B**, when the Vg-Id curve at the sweep from -20 V to +20 V is compared to the Vg-Id curve at the sweep from +20 V to -20 V, there is a particularly large difference (Δ shift) in a rising portion of the Vg-Id curves. The transistor characteristics in such a rising portion are important particularly in a device which is greatly affected by the value of off-state current. The shift value, which is one characteristic value of a transistor in a rising portion, means a voltage value at a rising of the Vg-Id curve and corresponds to a voltage at a drain-source current (I_d) of 1×10^{-12} A.

The following mechanism was assumed as a cause of the hysteresis characteristics.

A combination of light irradiation and application of a negative gate voltage induces a hole in the In—Ga—Zn—O-based oxide semiconductor (particularly in a vicinity of the interface with the gate insulating film). If a trap for capturing a hole exists in the bandgap, the hole is captured and remains in the vicinity of the interface with the gate insulating film as a positive charge, which causes a shift of the Vg-Id curve in the negative direction.

The sweep from -20 V to +20 V shifts the curve in the negative direction with a captured hole remaining in the vicinity of the interface due to the negative gate voltage. On the other hand, the sweep from +20 V to -20 V does not shift

the curve in the negative direction because a hole is excluded by the positive gate voltage. The difference in the hysteresis characteristics depending on the sweep speed between FIGS. **1A** and **1B** is affected by the reaction speed of a hole and a trap. In an oxide semiconductor, the reaction speed between a hole and a trap is very slow; a hole generated by light irradiation takes a long time to be captured, and once captured, the hole also takes a long time to be released.

To confirm the above-described assumed mechanism, verification using device simulation was conducted. For the simulation, a device simulator “Atlas” produced by Silvaco, Inc. was used.

Main parameters adopted in the simulation are listed in Table 2.

TABLE 2

Temperature	300 K
Bandgap	3.15 eV
Electronic affinity	4.3 eV
Permittivity	10
Mobility (electron)	10 cm ² /Vs
Work function (S/D)	4.0 eV
Work function (gate)	4.9 eV

Further, formulae of a recombination model adopted in the simulation are shown in Formula 1 and Formula 2.

$$R = \frac{pn - n_i^2}{\tau_n \left[p + n_i \exp\left(\frac{E_i - E_{trap}}{kT}\right) \right] + \tau_p \left[n + n_i \exp\left(\frac{E_{trap} - E_i}{kT}\right) \right]} \quad (\text{Formula 1})$$

$$\tau_n = \tau_p = 1.0 \text{ msec} \quad (\text{Formula 2})$$

For the simulation, a transistor whose structure is the same as that of the above-described measured transistor was hypothesized and traps as shown in FIGS. **6A** to **6D** were assumed in the bandgap of the In—Ga—Zn—O-based oxide semiconductor. No trap is included in the bandgap of FIG. **6A**, and a donor trap (trap for capturing a hole) is included in the bandgap in each of FIGS. **6B** to **6D**. FIGS. **6B** to **6D** are different in the energy difference from the valence band (E_v) to the trap. The simulation results are shown in FIGS. **7A-1** and **7A-2**, **7B-1** and **7B-2**, **7C-1** and **7C-2**, and **7D-1** and **7D-2**. The simulation results of Fast Sweep and Slow Sweep of FIG. **6A** are FIGS. **7A-1** and **7A-2**, respectively. The simulation results of Fast Sweep and Slow Sweep of FIG. **6B** are FIGS. **7B-1** and **7B-2**, respectively. The simulation results of Fast Sweep and Slow Sweep of FIG. **6C** are FIGS. **7C-1** and **7C-2**, respectively. The simulation results of Fast Sweep and Slow Sweep of FIG. **6D** are FIGS. **7D-1** and **7D-2**, respectively. It can be seen from the verification results that in the cases where the presence of a donor trap was assumed as an in-gap level, the hysteresis characteristics observed in the measurement results reappeared. It was also confirmed that in the cases where the trap exists near the valence band (FIGS. **6B** and **6C**), the hysteresis characteristics tend to be small. It can be assumed that this is because a captured hole is easily detrapped into the valence band even at a low temperature such as room temperature.

Further, as a cause of the difference in the hysteresis characteristics depending on the sweep speed in the measurement results, the following mechanism can be given: the reaction speed between a hole and a trap is very slow, and a hole generated by light irradiation takes a long time to be captured,

and once captured, the hole also takes a long time to be released. In the simulation of this embodiment, τ_n and τ_p in the Formula 2 were set to high values. In this manner, the tendency of the measurement results reappeared.

Finally, a donor level is considered below. An oxygen defect is given as an example of a defect level of a layer of an oxide semiconductor typified by an In—Ga—Zn—O-based oxide semiconductor. It is considered that electrons are localized in the case where vacancy owing to an oxygen defect is left. The state density of an oxygen-deficient state with oxygen vacancy left in an In—Ga—Zn—O-based oxide semiconductor is shown in FIG. 8. Simulation thereof was performed using Vienna Ab-initio Simulation Package (VASP), from which it can be found that the oxygen defect with vacancy left forms a deep level. In that case, the defect level is occupied with electrons and captures a hole because the defect level is close to the valence band. This defect level corresponds to the donor level capturing a hole assumed in the simulation.

FIG. 9 shows threshold changes (ΔV_{th}) of transistors in good results of a -BT test. Sample 3 is a transistor with the highest reliability among Samples 1, 2, and 3. Also for these transistors, with the V_g -Id measurement with light irradiation, results of which correlate with results of a -BT test, and thus, whether the reliability of each transistor is good or not good can be judged using the hysteresis characteristics. Negative-bias temperature stress photodegradation is a phenomenon in which a long period of stress application makes it impossible to detrapp trapped holes from the trap, and is caused by hole trapping, like the hysteresis characteristics. Therefore, according to the V_g -Id measurement with light irradiation, the sample with the smallest change is Sample 3 among Samples 1, 2, and 3, which coincides with the results of the -BT test.

Good/Not-Good judgment using hysteresis characteristics with the Id- V_g measurement is efficient in a shorter period of measurement than a BT test.

Embodiment 2

In Embodiment 2, an example of the case where a test using hysteresis characteristics is performed in a manufacturing process of a semiconductor device will be described.

An example of the manufacturing method of the transistor 410 is described using FIG. 2, below.

First, the insulating layer 420 serving as a base insulating layer is formed over the substrate 400. As the insulating layer 420, an insulating film including an inorganic insulating material is formed by a sputtering method, a PCVD method, or the like. Typically, an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or a gallium oxide film can be used as the insulating layer 420.

Although there is no particular limitation on a material and the like of the substrate 400, it is necessary that the substrate have heat resistance high enough to withstand at least a heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used as the substrate 400. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, carbon silicon, or the like; a compound semiconductor substrate of silicon germanium or the like; an SOI substrate; or the like can be used. Any of these substrates over which a semiconductor element is provided may be used as the substrate 400.

A flexible substrate may be used as the substrate 400. In the case where a transistor is provided over the flexible substrate,

the transistor may be formed directly on the flexible substrate, or the transistor may be formed over a different substrate and then separated to be transferred to the flexible substrate. In order to separate the transistor to transfer to the flexible substrate, a separation layer is preferably formed between the different substrate and the transistor.

Next, the gate electrode 401 is formed over the insulating layer 420. The gate electrode 401 can be formed to have a single-layer structure or a multi-layer structure using a metal material such as Mo, Ti, Cr, Ta, W, Al, Cu, Nd or Sc, and/or an alloy material containing the above metal material as its main component.

Then, the gate insulating layer 402 covering the gate electrode 401 is formed. The thickness of the gate insulating layer 402 is greater than or equal to 100 nm and less than or equal to 500 nm; for example, a first gate insulating layer having a thickness greater than or equal to 50 nm and less than or equal to 200 nm and a second gate insulating layer having a thickness greater than or equal to 5 nm and less than or equal to 300 nm are stacked in this order.

As the gate insulating layer 402, an insulating film including an inorganic insulating material is formed by a sputtering method, a PCVD method, or the like. Typically, an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or a gallium oxide film can be used as the gate insulating layer 402. In this embodiment, a 30-nm-thick silicon oxynitride film is formed.

Then, an oxide semiconductor film is formed to a thickness greater than or equal to 5 nm and less than or equal to 200 nm over the gate insulating layer 402. In this embodiment, the oxide semiconductor film is formed using a target for deposition of an oxide semiconductor, which contains In, Ga, and Zn (In_2O_3 : Ga_2O_3 : ZnO is 1:1:2 in molar ratio) under conditions where the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct current (DC) power is 5 kW, the atmosphere is an oxygen atmosphere (the proportion of the oxygen flow is 50%), and the substrate temperature is 200° C.

Next, the oxide semiconductor film is processed into the island-shaped oxide semiconductor layer 403 by a photolithography process.

Next, the oxide semiconductor layer 403 is dehydrated or dehydrogenated. First heat treatment for dehydration or dehydrogenation is performed at a temperature higher than or equal to 400° C. and lower than a strain point of the substrate, preferably higher than or equal to 425° C. In this embodiment, heat treatment is performed at 650° C. for 6 minutes, and then, heat treatment is performed at 450° C. for 1 hour in an atmosphere in which nitrogen and oxygen are mixed.

The heat treatment for dehydration or dehydrogenation of the oxide semiconductor layer may be performed on the oxide semiconductor film which has not been processed into the island-shaped oxide semiconductor layer. In that case, the substrate is taken out of the heat treatment apparatus after the heat treatment; then, a photolithography process is performed thereon.

Next, a conductive film is formed over the gate insulating layer 402 and the oxide insulating layer 403. Then, a resist mask is formed by a photolithography process, and selective etching is performed thereon to form the source electrode 405a and the drain electrode 405b. The source electrode 405a and the drain electrode 405b each can be formed to have a single-layer structure or a multi-layer structure using a metal material such as Mo, Ti, Cr, Ta, W, Al, Cu, Nd or Sc, and/or an alloy material containing the above metal material as its main component.

In this embodiment, two transistors are manufactured: Sample A in which a 200-nm-thick titanium (Ti) film is used as each of the source electrode **405a** and the drain electrode **405b**; Sample B in which a 200-nm-thick tungsten (W) film is used as each of the source electrode **405a** and the drain electrode **405b**.

Next, the resist mask is removed, and then, heat treatment is performed thereon at 300° C. for 1 hour in a nitrogen atmosphere.

Next, the buffer layer **407** covering the transistor **410** is formed. The buffer layer **407** is formed to have a single-layer structure or a multi-layer structure of an insulating film using an inorganic insulating material, an insulating film using an organic insulating material, or the like by a sputtering method, a PCVD method, or the like. As the buffer layer **407**, an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or a gallium oxide film, and/or an organic insulating film of an acrylic resin, a polyimide resin, or the like can be used. In this embodiment, a multi layer of a 300-nm-thick silicon oxide film formed by a sputtering method and a 1.5-μm-thick acrylic resin film is used as the buffer layer **407**.

Next, though not shown in FIG. 2, contact holes are formed in the buffer layer and connection electrodes which are connected to the source electrode **405a** and the drain electrode **405b** are formed.

Next, with light irradiation at 36000 lx with a white LED (manufactured by Moritex Corporation, a direct-below-type backlight MDBL-CW100), Vg-Id measurement is performed using as terminals the connection electrodes connected to the source electrode **405a** and the drain electrode **405b**. The light irradiation to the transistor **410** is performed as illustrated in FIG. 2.

The Vg-Id measurement was performed while irradiating the two transistors which are different in the materials of the source electrode **405a** and the drain electrode **405b**, with light, and the Vg-Id curve at a sweep from -6 V to +6 V by 0.25 V was compared to the Vg-Id curve at a sweep from +6 V to -6 V by 0.25 V.

As for the measurement of Sample A in which the Ti film is used as the material of the source electrode **405a** and the drain electrode **405b**, results of the measurement in which the integration time for one step (0.25 V) was set short to change the gate voltage fast (Fast Sweep) are shown in FIG. 4A, and results of the measurement in which the integration time for one step was set long to change the gate voltage slowly (Slow Sweep) are shown in FIG. 4B. The sweep rates of the Fast Sweep and the Slow Sweep are as listed in Table 1. The value of ΔShift in FIG. 4A was 1.0 V and the value of ΔShift in FIG. 4B was 2.4 V.

As for the measurement of Sample B in which the W film is used as the material of the source electrode **405a** and the drain electrode **405b**, results of the measurement in which the integration time for one step (0.25 V) was set short to change the gate voltage fast (Fast Sweep) are shown in FIG. 5A, and results of the measurement in which the integration time for one step was set long to change the gate voltage slowly (Slow Sweep) are shown in FIG. 5B. The value of ΔShift in FIG. 5A was 0.7 V and the value of ΔShift in FIG. 5B was 1.8 V.

The size of the transistor **410** is L/W=3 μm/50 μm.

Comparing Sample A to Sample B, the Vg-Id curve of Sample A using the Ti film was further shifted in a negative direction.

Further, results of a -BT test on Samples A and B are shown in FIGS. 4C and 5C, respectively. These results show correlation between the result of a -BT test and the result of

hysteresis characteristics. The value of ΔShift in FIG. 4C was 0.9 V and the value of ΔShift in FIG. 5C was 0.6 V.

In this manner, the Vg-Id characteristics of a transistor are measured while irradiating the transistor with light and a Good/Not-Good test is performed on the transistor, and then, the tested transistor can be included in an end-product such as a liquid crystal display device or a semiconductor chip. Without performing a BT test, a Good/Not-Good test can be performed on a transistor in a short period of time, and the transistor can be included in an end-product; accordingly, an electronic device with high reliability can be manufactured efficiently.

This application is based on Japanese Patent Application serial No. 2010-145410 filed with Japan Patent Office on Jun. 25, 2010, the entire content of which is hereby incorporated by reference.

What is claimed is:

1. A method for evaluating a hole trap level in a semiconductor, comprising:

manufacturing a transistor using the semiconductor as a channel region, the transistor comprising a gate electrode, a source electrode and a drain electrode;

obtaining a first Id-Vg curve of the transistor by measuring Id with increasing Vg from a negative value to a positive value at a first sweep rate under irradiation of light;

obtaining a second Id-Vg curve of the transistor by measuring Id with decreasing Vg from the positive value to the negative value at the first sweep rate under irradiation of light;

obtaining a third Id-Vg curve of the transistor by measuring Id with increasing Vg from the negative value to the positive value at a second sweep rate under irradiation of light;

obtaining a fourth Id-Vg curve of the transistor by measuring Id with decreasing Vg from the positive value to the negative value at the second sweep rate under irradiation of light; and

analyzing characteristics of the first Id-Vg curve, the second Id-Vg curve, the third Id-Vg curve and the fourth Id-Vg curve of the transistor,

wherein Vg is a voltage between the gate electrode and the source electrode of the transistor, and Id is a current between the drain electrode of the transistor and the source electrode, and

wherein the first sweep rate is different from the second sweep rate.

2. A method for evaluating a hole trap level in a semiconductor, comprising:

manufacturing a transistor using the semiconductor as a channel region, the transistor comprising a gate electrode, a source electrode and a drain electrode;

obtaining a first Id-Vg curve of the transistor by measuring Id with increasing Vg from a negative value to a positive value at a first sweep rate under irradiation of light;

obtaining a second Id-Vg curve of the transistor by measuring Id with decreasing Vg from the positive value to the negative value at the first sweep rate under irradiation of light;

obtaining a third Id-Vg curve of the transistor by measuring Id with increasing Vg from the negative value to the positive value at a second sweep rate under irradiation of light; and

obtaining a fourth Id-Vg curve of the transistor by measuring Id with decreasing Vg from the positive value to the negative value at the second sweep rate under irradiation of light,

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wherein a voltage between the gate electrode and the source electrode of the transistor is V_g , and a current between the drain electrode of the transistor and the source electrode is I_d , and

wherein the first sweep rate is different from the second sweep rate. 5

3. A method for manufacturing a device, comprising: manufacturing a transistor using a semiconductor as a channel region, the transistor comprising a gate electrode, a source electrode and a drain electrode;

obtaining a first I_d - V_g curve of the transistor by measuring I_d with increasing V_g from a negative value to a positive value at a first sweep rate under irradiation of light;

obtaining a second I_d - V_g curve of the transistor by measuring I_d with decreasing V_g from the positive value to the negative value at the first sweep rate under irradiation of light;

obtaining a third I_d - V_g curve of the transistor by measuring I_d with increasing V_g from the negative value to the positive value at a second sweep rate under irradiation of light;

obtaining a fourth I_d - V_g curve of the transistor by measuring I_d with decreasing V_g from the positive value to the negative value at the second sweep rate under irradiation of light; and 10

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subsequently manufacturing the device, using the transistor,

wherein V_g is a voltage between the gate electrode and the source electrode of the transistor, and I_d is a current between the drain electrode of the transistor and the source electrode, and

wherein the first sweep rate is different from the second sweep rate.

4. The method according to claim 1, wherein the semiconductor is an oxide.

5. The method according to claim 2, wherein the semiconductor is an oxide.

6. The method for manufacturing a device according to claim 3, wherein the semiconductor is an oxide.

7. The method according to claim 1, wherein the semiconductor is In—Ga—Zn—O-based oxide.

8. The method according to claim 2, wherein the semiconductor is In—Ga—Zn—O-based oxide.

9. The method for manufacturing a device according to claim 3, wherein the semiconductor is In—Ga—Zn—O-based oxide. 15

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